REMARKS/ARGUMENTS

1. Introduction

This is a full and timely response to the Office action of January 05, 2007. Claim 1 has been amended and new claims 41-42 dependent thereon are introduced. New claims 41-42 comprise limitations removed from claim 1 in this response and are supported at least by the pre-amended claim 1. No new material has been added. Reconsideration of all claims in the present application is respectfully requested.

2. Background

Claims 1, 4-7, 9-15, 17-25, and 27-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaku et al., US Patent 6,414,932, in view of Kato et al., US Patent 6,775,217 in view of Han, US Patent 7,102,976. Claims 8 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaku et al. in view of Kato et al. in view of Han, and further in view of Chung et al., US Patent 4,873,680.

3. Response

Claims 1, 19, and 40 each comprise the limitations of "the rough delay unit for generating a fine delay parameter according to the selected set of write strategy parameters".

If understood correctly, the Examiner suggests that the delay of the Kaku et al. element 104 corresponds to the present rough delay unit. However, as stated by the Examiner at the top of page 4 of the current Office action, Kaku et al. fails to disclose the fine delay chain, thus Kaku cannot anticipate the present rough delay unit generating a fine delay parameter.

Furthermore, although Kato et al. teaches both a rough delay unit and a fine delay unit, the fine delay parameter (N2) is generated by the write strategy delay table 350, not by the rough delay unit, and thusly Kato also fails to disclose the above limitations.

Claims 1, 19, and 40 each comprise the limitations of "the fine delay chain having a plurality of serially connected delay cells, each delay cell delaying the first delay signal by a predetermined period".

If understood correctly, the Examiner suggests that Kato et al. discloses a "plurality of serially connected delay cells" in Fig.5. But according to Col. 6, lines 1-3, Fig. 5 is a block diagram of the ring oscillator comprising the multi-phase clock synthesizer 320 of Fig. 3. Thus the element in Fig.5 is not part of the fine delay unit (324), but should be a multi-phase clock synthesizer (320). Therefore neither Kaku et al. nor Kato et al. teach this limitation.

Additionally, concerning at least claim 40, on page 5 of the current Office action, if understood correctly, the Examiner suggests Col.5, lines 29-40 of Kato et al. teach how delay parameters can be generated without the use of a clock signal and thusly anticipates claim 40 limitations of "wherein the fine delay chain is not connected to and does not utilize a clock signal for delaying the first delay signal to generate the write signal."

It is agreed that Col.5, lines 29-40 of Kato et al. may be considered as teaching a possibility of generating delay parameters without the use of a clock. However, the cited claim 40 limitations do not pertain to generating delay parameters, but instead to **not utilizing a clock signal for delaying** the first delay signal to generate the write signal. There is a difference between generation and utilization.

On the page 4 of the current Office action and still referring to Kato et al., the Examiner states: "the differential amplifiers of figure 5 serve this purpose as is explained in column 6, lines 1-10" and uses this citation to anticipate the claim 40 limitations of "the fine delay chain comprising a plurality of serially connected delay cells".

The applicant asserts that if Kato et al.'s ring oscillator 500 (Examiner cited Fig.5 and Col.6, lines 1-10) is utilized to anticipate limitations of the present "fine delay chain", then the ring oscillator 500 must be connected to a clock (Fig.5, Fig.3, Col.6, lines 1-10) or it will fail to function making it an unobvious modification. On the other hand, if the Examiner is suggesting that Kato et al. teaches that the fine

delay unit is somehow not connected to a clock, then the ring oscillator cannot be used to anticipate the claim 1, 19, and 40's limitation of "plurality of serially connected delay cells". Kato et al., alone or in combination with other known art cannot anticipate both limitations.

3. Summary

The difference between Kato et al. and the current disclosure is that the current fine delay of this invention uses the delay cells to generate a plurality of write signals, then uses the multiplexer to select an output from the generated write signals according to the fine delay parameter. Each delay cell delays the first delay signal by a predetermined period.

Kato selects a clock from a plurality of multi-phase clocks to delay the first delay signal according to the fine delay parameter.

Thus Kato has a more complicated layout (more multi-phase clocks are required for higher resolution). The present disclose does not need multi-phase clocks, thus is simplified in structure and operation. Additionally, Kato et al.'s fine delay cannot combine a plurality of delay cells because the associated specification fails to teach how to combine multi-phase clocks with delay cells. A person skilled in the art does not have the knowledge to reasonably combine the multiple clocks and multiple delay cells to generate the function of the present fine delay unit.

For at least these reasons, the applicant respectfully requests reconsideration of independent claims 1, 19, and 40. While retaining all rights for a future response to Examiner comments concerning these and other claims in the application, inasmuch as the allowability of dependent claims ultimately rests upon the allowability of their respective base claims, reconsideration of dependent claims 4-15, 17-18, 20-39, and 41-42 is respectfully requested.

Sincerely yours,

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